Claim Amendments

1. (canceled without prejudice) ~~An apparatus for adding a plurality of partial products comprising:~~

~~a plurality of carry-save adders coupled together in series, each of the carry-save adders in the series receiving one of the plurality of partial products and two intermediate vectors from a prior carry-save adder in the series of carry-save adders, and outputting a carry bit, a sum bit and two intermediate vectors, wherein the first one in the series of carry-save adders receives two of the plurality of partial products;~~

~~a last carry-save adder coupled to a last one in the series of carry-save adders and receiving a last partial product of the plurality of partial products and two intermediate vectors from a last one in the series of carry-save adders, and outputting a carry vector (Cmsb) and a sum vector (Smsb);~~

~~a plurality of carry-propagate adders coupled in series and coupled to the plurality of carry-save adders, each of said plurality of carry-propagate adders outputting a resulting bit and a carry bit; and~~

~~an output register coupled to the first one in the series of carry-save adders, the last carry-save adder, and the plurality of carry-propagate adders, and storing the plurality of resulting bits, the sum bit output by the first one in the series of carry-save adders and the carry bit output by the last one in the series of carry-propagate adders.~~

2. (canceled without prejudice) ~~The apparatus according to claim 1, further comprising:~~

~~a MOST SIGNIFICANT BIT carry output register coupled to the last carry-save adder and storing the most significant bit carry vector (Cmsb); and~~

~~a MOST SIGNIFICANT BIT sum output register coupled to the last carry-save adder and storing the most significant bit sum vector (Smsb).~~

3. (canceled without prejudice) ~~The apparatus according to claim 1, wherein at least one of the carry-propagate adders comprises a half-adder and the other carry-propagate adders comprise full-adders~~.

4. (canceled without prejudice) ~~An apparatus for adding a plurality of partial products comprising:~~

~~a plurality of carry-save adders coupled together in series, each of the plurality of carry-save adders receiving a successive one of the plurality of partial products and two intermediate vectors (In-1, In-2) from a prior carry-save adder in the series of carry-save adders and each of the plurality of carry-save adders outputting a carry bit (Cn-1) a sum bit (Sn-1) and two intermediate vectors (In, In+1) wherein a first one in the series of carry-save adders receives two of the plurality of partial products;~~

~~a last carry-save adder coupled to a last one in the series of carry-save adders, receiving a last one of the plurality of partial products and two intermediate vectors from said last one in the series of carry-save adders, and outputting a plurality of sum bits and a plurality of carry bits; and~~

~~a plurality of half-adder/full-adder series combinations coupled to the last carry-save adder, each of the plurality of half-adder/full-adder series combinations receiving two carry bits of the plurality of carry bits output by the last carry-save adder and two sum bits of the plurality of sum bits output by the last carry-save adder, and outputting two result bits and a carry bit~~.

5. (currently amended) ~~The apparatus according to claim 4, further comprising:~~

An apparatus for adding a plurality of partial products comprising:

a plurality of carry-save adders coupled together in series, each of the plurality of carry-save adders receiving a successive one of the plurality of partial products and two intermediate vectors (In-1, In-2) from a prior carry-save adder

in the series of carry-save adders and each of the plurality of carry-save adders outputting a carry bit (Cn-1) a sum bit (Sn-1) and two intermediate vectors (In, In+1) wherein a first one in the series of carry-save adders receives two of the plurality of partial products;

a last carry-save adder coupled to a last one in the series of carry-save adders, receiving a last one of the plurality of partial products and two intermediate vectors from said last one in the series of carry-save adders, and outputting a plurality of sum bits and a plurality of carry bits;

a plurality of half-adder/full-adder series combinations coupled to the last carry-save adder, each of the plurality of half-adder/full-adder series combinations receiving two carry bits of the plurality of carry bits output by the last carry-save adder and two sum bits of the plurality of sum bits output by the last carry-save adder, and outputting two result bits and a carry bit;

two half-adders coupled together in series and coupled to the last carry-save adder, said two half-adders receiving from the last carry-save adder two most significant carry bits and a most significant sum bit and outputting two result bits and a carry bit as a plurality of most significant bits of the result of adding the plurality of partial products.

6. (previously amended) The apparatus according to claim 5, further comprising

a single output register coupled to the plurality of half-adder/full-adder combinations and storing the two result bits and the carry bit output by each of the plurality of half-adder/full-adder series combinations.

7. (currently amended) A method of reducing the speed of a multiplier comprising the step of:

replacing carry and save registers ~~[49a, 49b]~~ relating to a set of least significant bits with a single register ~~[48]~~ and a carry-propagate adder comprising a half adder ~~[37]~~ and a set of full adders ~~[38-40]~~.